

December 15, 2009

Analysis of scratches formed on oxide surface during chemical mechanical planarization

Jae-Gon Choi

Hanyang University - Dept. of Materials Engineering ; Hanyang University - Dept. of Bio-Nano Technology ; FAB Technology, Korea - Hynix Semiconductor Incorporated, Memory Research and Development Division

Y. Nagendra Prasad

Hanyang University - Dept. of Materials Engineering

In-Kwon Kim

Hanyang University - Dept. of Materials Engineering

In-Gon Kim

Hanyang University - Dept. of Bio-Nano Technology

Woo-Jin Kim

FAB Technology, Korea - Hynix Semiconductor Incorporated, Memory Research and Development Division

See next page for additional authors

Recommended Citation

Choi, Jae-Gon; Prasad, Y. Nagendra; Kim, In-Kwon; Kim, In-Gon; Kim, Woo-Jin; Busnaina, Ahmed A.; and Park, Jin-Goo, "Analysis of scratches formed on oxide surface during chemical mechanical planarization" (2009). *Center for High-Rate Nanomanufacturing Publications*. Paper 20. <http://hdl.handle.net/2047/d20000966>

Author(s)

Jae-Gon Choi, Y. Nagendra Prasad, In-Kwon Kim, In-Gon Kim, Woo-Jin Kim, Ahmed A. Busnaina, and Jin-Goo Park



Analysis of Scratches Formed on Oxide Surface during Chemical Mechanical Planarization

Jae-Gon Choi,^{a,c} Y. Nagendra Prasad,^a In-Kwon Kim,^a In-Gon Kim,^b
Woo-Jin Kim,^c Ahmed A. Busnaina,^d and Jin-Goo Park^{a,b,*z}

^aDepartment of Materials Engineering and ^bBio-Nano Technology, Hanyang University, Ansan 426-791, Korea

^cHynix Semiconductor Incorporated, Memory Research and Development Division, FAB Technology, Icheon 467-701, Korea

^dNSF Center for Microcontamination Control, Northeastern University, Boston, Massachusetts 02115, USA

Scratch formation on patterned oxide wafers during the chemical mechanical planarization process was investigated. Silica and ceria slurries were used for polishing the experiments to observe the effect of abrasives on the scratch formation. Interlevel dielectric patterned wafers were used to study the scratch dimensions, and shallow trench isolation patterned wafers were used to study the effect of polishing parameters, such as pressure and rotational speed (head/platen). Similar shapes of scratches (chatter type) were observed with both types of slurries. The length of the scratch formed might be related to the period of contact between the wafer and the pad. Large particles would play a significant role in increasing the number of scratches. The probability of scratch generation is more at higher pressures due to higher friction force and removal rate. The optimization of the head to platen velocity could decrease the number of scratches.

© 2009 The Electrochemical Society. [DOI: 10.1149/1.3265474] All rights reserved.

Manuscript submitted August 10, 2009; revised manuscript received October 26, 2009. Published December 15, 2009.

Planarization of the oxide surface is a critical process during interlevel dielectric (ILD) formation and shallow trench isolation (STI) processes. During both processes, chemical mechanical planarization (CMP) is a key technology to planarize the oxide surface.¹⁻⁵ Various defects, such as organic residues, surface particles, dishing, erosion, and scratches, would be produced during the CMP process, but the most detrimental defect would be scratch formation.^{6,7} The other types of defects produced could be removed by other means during post-CMP cleaning, but the removal of a scratch is not an easy task.⁸ In the ILD CMP process, the scratches on an oxide film surface directly affect the yield and reliability of devices.⁹ The scratches formed during the STI CMP process would create the problem during gate oxide integrity in semiconductor production.^{3,5}

Much research has been done on studying the methods of scratch reduction by controlling different polishing conditions and consumable parts,^{3-6,9,10} but understanding the origins of the scratches generated on pattern wafers during real-time polishing has not been discussed. In a CMP process, consumable parts, such as a slurry, a polishing pad, and a diamond conditioning disk, can cause surface scratches. Incorporating the mentioned consumables to a CMP process, numerous root causes have been discussed: agglomeration of abrasive particles,^{2,4,11,12} hard abrasives with large and polydisperse size and shape,^{13,14} improper contact of abrasive particles on the wafer surface,¹⁵ pad conditioning,¹¹ polishing pad debris, slurry by-products/residue, conditioning methods,^{16,17} etc. Among them, the major sources were the presence of large particles or the agglomeration of slurry particles during the process. Therefore, most of the CMP processes rely heavily on the application of fine point-of-use filters^{2,4} to remove and reduce scratch sources from the slurry, but the CMP scratch issue is still the most serious defect issue.

In this study, the effect of the nature of abrasives and process conditions on the scratch formation was studied during oxide CMP. Silica and ceria slurries are the most commonly used slurries for oxide CMP processes; hence, these slurries were used for the study. The scratch formation mechanism was explained in detail based on the shape and dimensions of the scratches. The effect of polishing pressure and rotational speed on several scratches formed was discussed.

Experimental

In this work, three types of oxide wafers were used: blanket oxide wafers, ILD patterned wafers, and STI patterned wafers. Tetraethyl orthosilicate (6000 Å) was deposited on blanket 200 mm Si wafers by high density plasma chemical vapor deposition (Novellus) and was used to measure the removal rate. Patterned wafers were used to detect the scratch formed during CMP because it would be very difficult to observe scratches on blanket oxide wafers. ILD patterned wafers were used for studying the scratch shape and its dimensions, such as length, width, lip width, and depth, because the scratches formed on these wafers would not be deformed but would be rigid enough to understand the formation mechanism of the scratches. The scratches on the wafer were observed by a dark-field patterned wafer inspection system (PUMA 9100, KLA-Tencor). A critical dimension-scanning electron microscope (CD-SEM, Hitachi), which is mostly used for the measurement of contact dimension after the mask and etch process, was employed for the analysis of each scratch shape, such as length, width, and lip width. The scratch depth was analyzed by a focused ion beam (FIB, FEI Strata 400S) and a transmission electron microscope (TEM, FEI CM 200).

STI patterned wafers were used to investigate the effect of process conditions, such as pressure and rotation speed, on scratch formation because the detection and counting of scratches are easy with these wafers due to the clear visibility of oxide and nitride with distinctive color when viewed through a field-emission SEM on STI patterns. The polishing pressure was varied from 2 to 6 psi, whereas the platen and head speeds were varied from 5 to 95 rpm such that the sum of these two velocities was set to 100 rpm as a reference to perform the experiments in an organized way. There is no technical importance for keeping 100 rpm as reference. The polishing experiments were carried out on a 200 mm polisher (Mirra, AMAT). The slurry flow rate was set at 200 mL/min, and the K-grooved IC-1010 pad (Dow Electronic Materials) was used for all polishing experiments. The film thicknesses of the blanket wafer and patterned wafers were measured before and after polishing by a reflectometer (NANO-Spec 9100, Nanometrics). The ILD and STI patterned wafers were polished with a commercial fumed silica slurry (12 wt %, Dongjin Semichem, Korea) and ceria slurry (5 wt %, Hitachi, Japan), which was mixed with deionized water and additives for selectivity between oxide and nitride films, respectively. The compositions of silica and ceria slurry were chosen based on their identical performance in terms of removal rate and nonuniformity. The pH values of silica and ceria slurry were 11 and 7, respectively. The

* Electrochemical Society Active Member.

^z E-mail: jgpark@hanyang.ac.kr

Table I. Physical characteristics of fumed silica and ceria slurries used for polishing.

Physical characteristics	Fumed silica	Ceria
Mean particle size	180–200	220–240
Hardness (Mohs)	6.0–7.0	—
Particle structure	Amorphous	Polycrystalline
point of zero charge (pH)	2.2	7
Density (g/cm ³)	2.2–2.6	7.13

mean particle size of silica and ceria was measured by TEM analysis. The typical physical characteristics of the two slurries are shown in Table I.

Results and Discussion

Figure 1a and b shows the top view SEM images of the ILD patterned wafers after CMP with fumed silica and ceria based slurries, respectively. Even though the physical properties of the fumed silica and ceria particles were different, the shape of the scratches formed by the fumed silica based slurry was similar to that of the scratches formed by the ceria based slurry. Both slurries generated

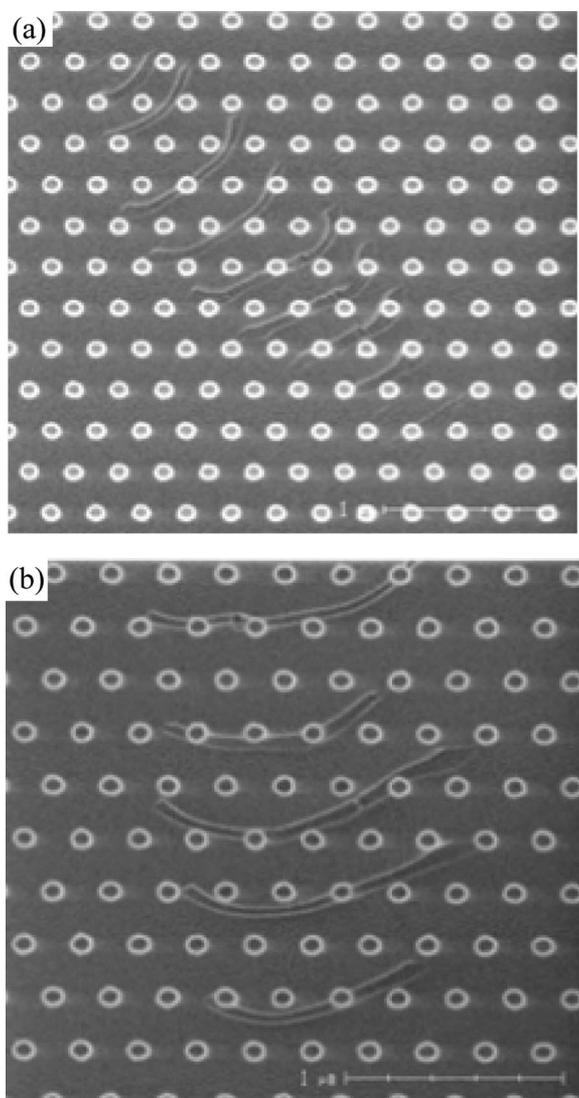


Figure 1. Top view of scratches after ILD CMP with (a) fumed silica slurry and (b) ceria slurry.

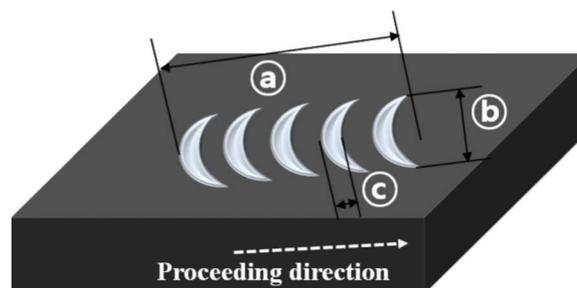


Figure 2. (Color online) Schematic illustration of ILD CMP scratch shape dimensions where (a) is the length of the scratch, (b) is the width of the scratch, and (c) is the lip width.

the caterpillar/chatter-mark-type scratches. Others also observed similar shapes of scratches on the oxide surface when polished with either the silica slurry or the ceria slurry.^{3,5,12} It was proposed that the chatter mark shape (eyebrow shape) might be due to the presence of abnormally large size abrasives in the incoming slurry or because of the agglomeration of the slurry particles by the heat produced during the process.¹² Also, Lee et al. claimed that the scratches formed by the ceria slurry might be due to the presence of a higher portion of large particles with a size of over 1.0 μm in the slurry.³ However, other works proposed that agglomeration of the particles is the most probable reason to produce the scratches.^{8,18} If agglomeration were the primary reason, then silica slurry should produce a higher number of scratches than ceria, but the frequency of scratches generated is much higher with ceria slurry than with silica slurry.^{3,19} The reason for this may be attributed to more hardness, typical angular morphology of the ceria particles than of the silica particles, and more importantly, a higher reactivity of ceria with the oxide surface.¹ So, it is the nature of the particle that causes more scratches than agglomeration. The chatter-mark-type microscratches might be related to “abrasive wear mechanism.”^{14,20} Ahmadi and Xia proposed a theory that when hard abrasive particles are immobilized between two sliding surfaces (wafer and pad), the abrasives might be adhered or embedded in one of the sliding surfaces and plow out grooves on the other surface.²⁰ It might also be speculated that some particles might have been trapped between the pad asperities to create chatter mark shape scratches because the contact time between the wafer and pad changed with their simultaneous movement. Because ceria has more chemical reactivity than silica with the oxide surface, the probability of the formation of scratches with ceria slurry would be higher.

To understand microscratch formation, all scratches were reviewed manually with trained eyes and were characterized thoroughly. The scratches were observed to be formed mostly as a group of segments on the surface, which would appear as chatter marks or eyebrows or caterpillar marks. A schematic diagram of a scratch (chatter mark type) formed on the substrate is shown in Fig. 2. The scratch dimensions could be classified into four parts: length, width, lip width, and depth. Lip width is defined as the width of a single segment. The length of the segment was considered as the length of the scratch, and it was measured by CD-SEM at a fixed magnification of $\times 20,000$. Figure 3a–c shows the distribution of dimensions (length, width, and lip width) of scratches formed after the ILD CMP process. The maximum, minimum, and mean values of the dimensions are shown in Table II. The majority of scratches formed were below 8 μm , and very few scratches were observed with lengths greater than 8 μm , but most of the scratch segments had $< 2 \mu\text{m}$ length, as shown in Fig. 3a. Here, one question that might be of interest is: What would the source and mechanism be to generate different lengths of scratches? It could be explained as follows: The possible sources for creating scratches would be the agglomerated particles, the debris from the pad, and the conditioner. Agglomerated particles would be weak scratch sources, whereas pad debris

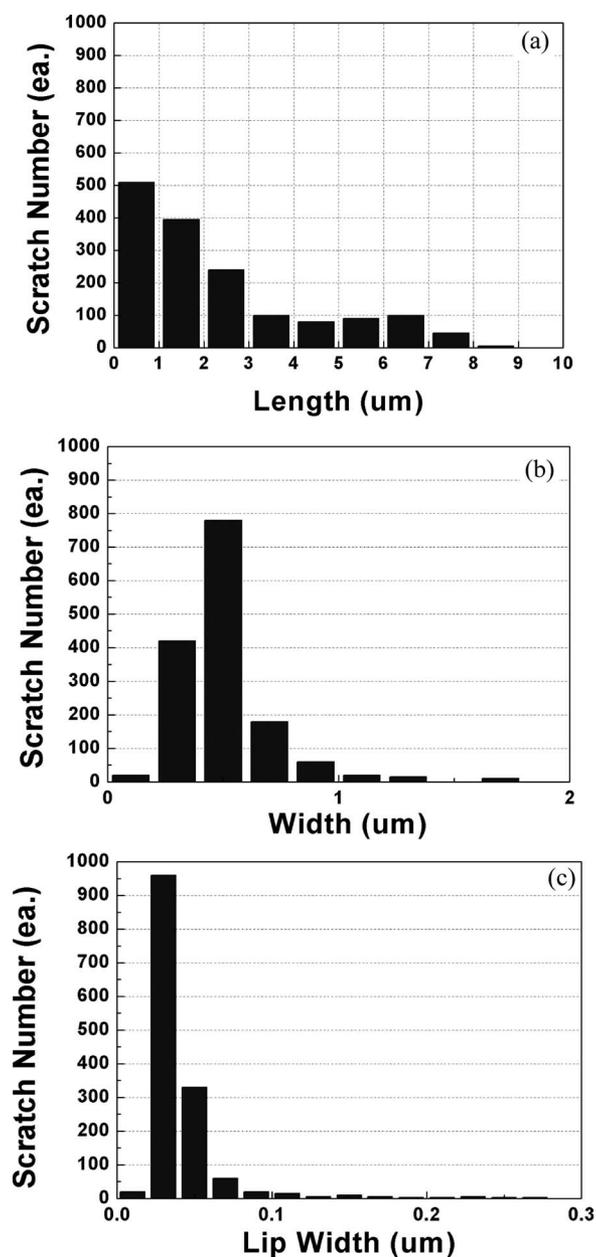


Figure 3. Distribution of dimensions of the number scratches after the ILD CMP with fumed silica slurry: (a) length, (b) width, and (c) lip width.

or conditioner debris would be the strong scratch sources during the CMP process. If one of the above were assumed to be the scratch source and impinged in between the wafer and the pad surface, then the length of the scratch would depend on the location of the impingement between the pad and wafer contact as well as the strength (feebler or firmer) of the scratch source. If the scratch source, either

Table II. The maximum, minimum, and mean values of scratch dimensions formed after ILD CMP by using silica slurry.

	Maximum	Minimum	Mean
Length (μm)	24.1	0.2	2.49
Width (μm)	6.64	0.03	0.53
Lip width (μm)	0.69	0.002	0.06
Depth (\AA)	1182	212	694

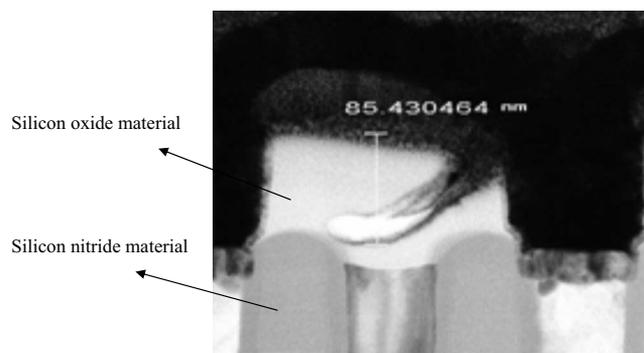


Figure 4. Cross-sectional FIB-TEM image of the depth of the scratch formed after ILD CMP process with silica slurry.

feebler or firmer, were generated at the outer edge (exit) of the wafer during the rotation, the source would have little time to come into contact with the wafer and would come out immediately from the wafer-pad contact after creating the small scratch on the wafer surface. Otherwise, if the source were generated at the middle of the wafer or at the entrance of the wafer during the rotation, two possibilities might exist, that is, either the source (if it were feebler) would be fractured, creating small scratches, or the source (if it were firmer) would be embedded in the polishing pad firmly during the polishing process. As a result, they might excavate a furrow on the surface. When the source was bumped from the pad and wafer interface, that would be the end of the scratch, which would resemble the abrasive wear mechanism, as discussed above.²⁰ If scratch sources were assumed to be the agglomerated slurry particles, this means that they would be broken by an external force, such as pressure, or come out from a pad surface after $<2 \mu\text{m}$ scratches were made. So, the smaller scratches may be attributed to the large or agglomerated particles, which would spend a short time between the wafer and the pad. The larger scratches more than $8 \mu\text{m}$ may be attributed to the scratch sources embedded firmly between the wafer and pad contact. It is shown in Fig. 3b that the width of most scratches was distributed in the range of $0.3\text{--}0.6 \mu\text{m}$. So, it was expected that the diameter of most scratch sources might be distributed in this range if the shape of the scratch sources were assumed to be a sphere. Figure 3c shows that over 90% of the scratches formed had lip widths of $0.02\text{--}0.04 \mu\text{m}$. From the observation of the scratch size and shape, it could be concluded that the scratch sources generated during polishing might be a thin flake with a width of about $0.06 \mu\text{m}$ and a diameter of about $0.5 \mu\text{m}$. It is difficult to measure the depth of the scratches when compared to other dimensions. For the depth measurements, small portions of total scratches were taken and observed by FIB-TEM, as shown in Fig. 4. The depths of the scratches were in the range of $212\text{--}1182 \text{\AA}$. The average depth was measured to be around 694\AA . The TEM image of the cross section of the depth of the scratch is shown in Fig. 4, and it shows that the scratch was developed vertically in the reverse direction of polishing platen rotation. The above analysis of scratch data might not be universal because the scratch would be influenced by the hardness of many materials, such as the underlying pattern material, scratch sources, and polished material.

The presence of large particles would increase the possibility of scratches.^{2,18,21-23} To examine the effect of large size particles on the scratch number, silica particles of $>1 \mu\text{m}$ were added to the commercial slurry for polishing the ILD patterned wafer. Different experiments were conducted with two types of silica slurries containing one with $>1 \mu\text{m}$ particles (sample 1) and another without $>1 \mu\text{m}$ particles (sample 2) by using a filter, as shown in Fig. 5. First, 30 polishing experiments were conducted with the slurry containing large size particles, and the remaining 20 experiments were conducted without adding large particles. From the results, it is obvious that slurry containing $>1 \mu\text{m}$ particles produced many

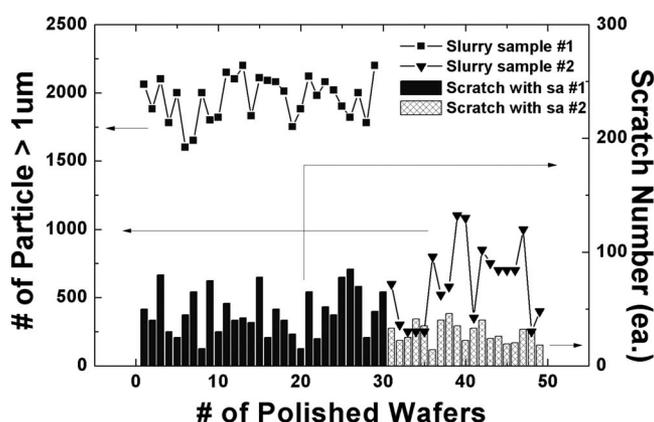


Figure 5. The correlation between the number of scratches produced by the slurries with and without large size particles.

scratches than that without $>1 \mu\text{m}$ particles. The average number of scratches formed per wafer were 49 and 26 with the slurries with and without the addition of large particles. This could be attributed to the fact that the role of large abrasives would be significant for scratch formation.² Even without the presence of the large particles, the number of scratches was significant on the polished surfaces. Other factors should not be ignored. Factors such as pressure and rotational speed were investigated to understand the scratch formation mechanism.

To study the impact of polishing parameters such as pressure and rotation speed, the STI patterned wafers were polished with ceria slurry to observe the scratch formation. The degree of contact in the pad-slurry interface could be understood by the Somerfield number (SN) in connection with the coefficient of friction (COF).²⁴ The scratch generation could be understood by examining the lubrication regime, which would describe the direct contact among the polishing pad, the slurry particle, and the wafer surface. Preston's equation states that the polishing rate is linearly proportional to the polishing pressure.²⁵ The variation in removal rate and COF as a function of pressure was studied on blanket oxide wafers due to a higher removal rate of oxide with ceria slurry and is shown in Fig. 6. It could be observed that the removal rate and COF were the linear functions of pressure. So, with an increase in pressure, both the removal rate and the COF would increase. An increased COF value would not mean an increase in the number of scratches, but it would mean an increase in the probability of scratch generation. With increasing polishing pressure, SN would be decreased according to Eq. 1.^{16,26,27}

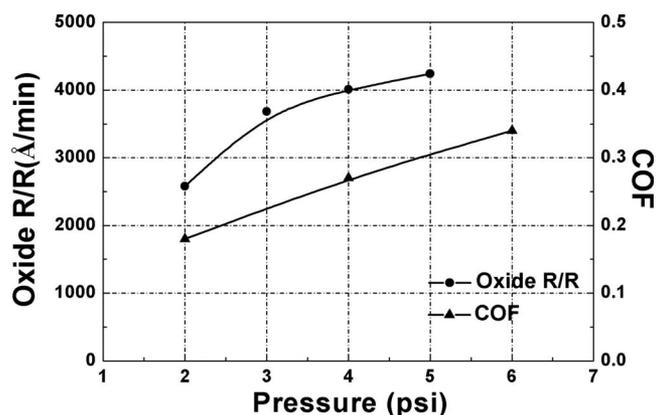


Figure 6. Friction force and removal rate of blanket oxide film as a function of pressure with ceria slurry.

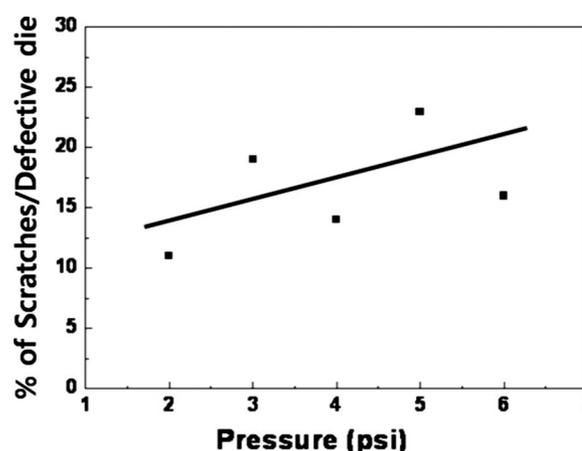


Figure 7. Number of scratches generated on oxide (STI patterned wafer) after polishing as a function of pressure.

$$\text{SN} = \frac{V \cdot \mu}{p \cdot \sigma_{\text{eff}}} \quad [1]$$

where V is the pad-wafer sliding velocity, p is the applied wafer pressure, μ is the slurry viscosity, and σ is the effective fluid film thickness between the pad and the wafer. From this equation, with increasing polishing pressure, SN would gradually decrease, but COF would increase. The relationship between SN and COF during the CMP process could be determined by the Stribeck-Gumbel curve.²⁷ From this curve, the boundary lubrication regime would describe the direct contact among the polishing pad, the slurry particles, and the wafer surface. The probability of scratch generation could be higher in this regime. Scratches formed were counted at different pressures by sampling the scratches formed per 100 defective dies of the wafer after the CMP process, as shown in Fig. 7. Though the fitting appeared to be forceful, the total number of scratches were increased with pressure under a manual observation. Though the number of scratches would increase with the increase in pressure, the exact relationship between pressure and number of scratches was not clear.

The effect of polishing speed on scratch formation was also studied by varying the platen and head speeds. In this study, the higher head speed condition compared to the platen speed was not studied because of the low polishing rate. Generally, the polishing rate is more sensitive to the platen speed because the diameter of the platen is about 50% larger than that of the polishing head in the polisher for device manufacturing. As shown in Fig. 8, the removal rate was decreased with decreasing platen speed; the more the platen speed decreases, the more the value at the x -axis (head/platen ratio) increases. As the removal rate was very low at a lower platen speed, polishing experiments at a higher platen rpm were only considered. Figure 9 shows the ratio of the number of scratches to the number of defects on a die as a function of relative speed between head and platen, where only the higher platen rpm was maintained. The number of scratches was not linearly proportional to the platen speed. However, the scratch number was too low at all higher platen speeds, and the trend should be considered constant. To further investigate it, the friction force was measured with relative rotation speed between head and platen speeds, as shown in Fig. 10, but did not change much at different head and platen rotation speeds. It could be ascertained that the trend of COF in Fig. 10 did not follow the trend of the removal rate in Fig. 8 because COF alone could not drive the changes in removal rate.²⁸⁻³⁰ It could be observed that the friction force was not directly related to the scratch formation by changing the platen and head rotation speeds. If the friction force does not explain the number of scratches formed by changing rotation speeds, this phenomenon could only be explained from the definition of the SN. The SN increases with the increase in rotation

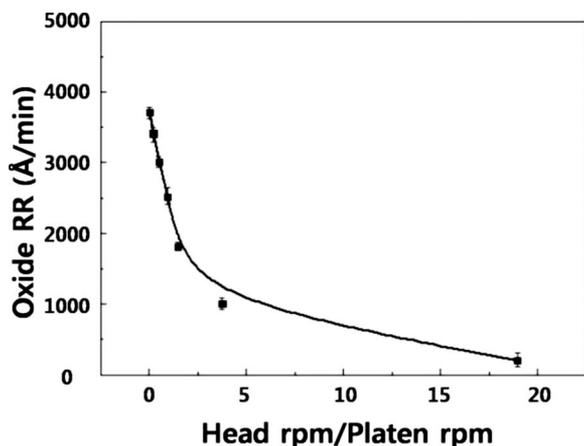


Figure 8. Removal rate of oxide with the ratio between head and platen speeds.

speed, so the lubrication status between the polishing pad and the wafer surface would be changed to an area in one of the three regimes in the Stribeck curve. From that result, the condition showed that the best result could be placed within the range of

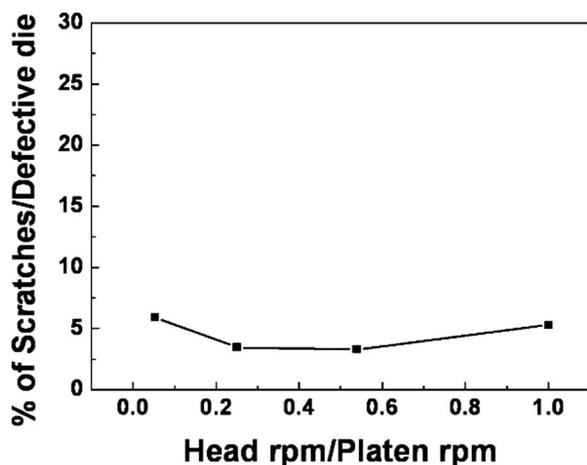


Figure 9. The variation in the ratio of scratch defect to total defect with an increase in the ratio between the head and platen speeds.

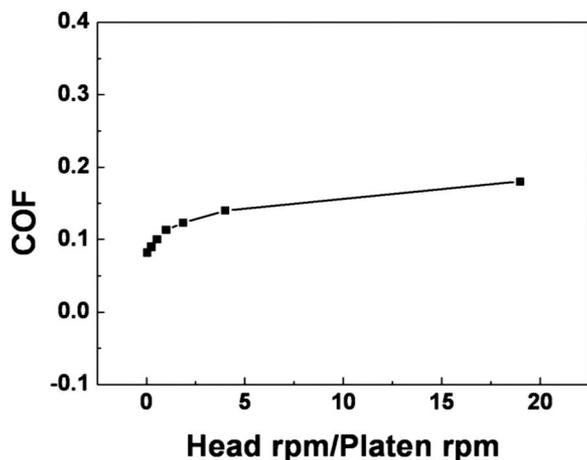


Figure 10. Friction force of blanket oxide film as a function of head/platen speed ratio.

hydrodynamic lubrication. The hydrodynamics determines the slurry film thickness, and then its film thickness depends on the average pad-wafer relative speed. Therefore, slurry film thickness is easily influenced by the platen speed. So, it would be expected that at lower platen speeds the possibility of scratches would be higher.⁸

Conclusions

In this study, the analysis of scratches formed on the oxide surface during the CMP process was investigated with patterned wafers using silica and ceria slurries. The shape of scratches, which was generated during ILD CMP, was very similar to the caterpillar type. Scratch dimensions such as length, width, lip width, and depth were characterized thoroughly on ILD patterned wafers, and the effect of polishing parameters on the scratch number was studied on STI patterned wafers. The variation in the length of the scratches would be dependent on the generation of the location of the scratch source and was explained based on the abrasive wear mechanism. Based on the scratch dimension measurements, it could be expected that the scratch source might be of a sphere shape in the form of a thin flake. The role of the large size abrasives would be significant for the scratch formation. So, the size and number of the large particles in the incoming slurry could be controlled to reduce the scratch formation. The effect of polishing pressure and rotation could be best understood from the Stribeck-Gumbel curve. The effect of pressure was not clear on the scratch numbers, but it could be regarded that the probability of scratch generation would be more at higher pressures. Based on the film thickness between wafer and pad, it would be expected that with the increase in platen velocity, the number of scratches would be reduced.

Acknowledgments

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (no. R11-2008-044-02004-0) and Hanyang University-Ansan Regional Innovation Center (HYRIC).

Hanyang University assisted in meeting the publication costs of this article.

References

1. Y. Li, *Microelectronic Applications of Chemical Mechanical Planarization*, John Wiley & Sons, Somerset, NJ (2008).
2. Y.-J. Seo, S. Y. Kim, Y.-O. Choi, Y.-T. Oh, and W.-S. Lee, *Mater. Lett.*, **58**, 2091 (2004).
3. S.-I. Lee, J. Hwang, H. Kim, and H. Jeong, *Microelectron. Eng.*, **84**, 626 (2007).
4. S.-Y. Kim, S.-W. Park, and Y.-J. Seo, *J. Mater. Sci.*, **13**, 693 (2002).
5. C. M. Chiu, T. F. Yen, and K.-F. Chiu, *J. Vac. Sci. Technol. B*, **21**, 960 (2003).
6. J. Y. Lin, A. C. West, C. C. Wan, and Y. Y. Wang, *Electrochem. Commun.*, **10**, 677 (2008).
7. J. G. Park and T. G. Kim, *Mater. Res. Soc. Symp. Proc.*, **991**, 53 (2007).
8. J. Tang, D. Dornfeld, S. K. Pangrle, and A. Dangca, *J. Electron. Mater.*, **27**, 1099 (1998).
9. Y. J. Seo, S.-Y. Kim, and W.-S. Lee, *Microelectron. Eng.*, **70**, 1 (2003).
10. Y. Ahn, J.-Y. Yoon, C.-W. Baek, and Y.-K. Kim, *Wear*, **257**, 785 (2004).
11. A. Chandra, P. Karra, A. F. Bastawros, R. Biswas, P. J. Sherman, S. Armini, and D. A. Lucca, *Anal. of the CIRP*, **57**, 559 (2008).
12. S.-M. Jung, J.-S. Uom, W.-S. Cho, Y.-J. Bae, Y.-K. Chung, K.-S. Yu, K.-Y. Kim, and K.-T. Kim, in *39th Annual International Reliability Physics Symposium*, Orlando, FL, IEEE, p. 42 (2001).
13. S. Armini, C. M. Whelan, K. Maex, J. L. Hernandez, and M. Moinpour, *J. Electrochem. Soc.*, **154**, H667 (2007).
14. T. Y. Teo, W. L. Goh, L. S. Leong, V. S. K. Lim, T. Y. Tse, and L. Chan, *Proc. SPIE*, **5041**, 61 (2003).
15. S.-K. Kim, Y.-H. Kim, U. Paik, T. Katoh, and J.-G. Park, *J. Electroceram.*, **17**, 835 (2006).
16. D. Denardis, Y. Seike, M. Takaoka, K. Miyachi, and A. Philipossian, *Wear*, **260**, 1224 (2006).
17. T. Ha, T. Miyoshi, Y. Takaya, and S. Takahashi, *Precis. Eng.*, **27**, 265 (2003).
18. E. E. Remsen, S. Anjur, D. Boldridge, M. Kamiti, S. Li, T. Johns, C. Dowell, J. Kasthurirangan, and P. Feeney, *J. Electrochem. Soc.*, **153**, G453 (2006).
19. S. Armini, C. M. Whelan, M. Moinpour, and K. Maex, *J. Electrochem. Soc.*, **155**, H653 (2008).
20. G. Ahmadi and X. Xia, *J. Electrochem. Soc.*, **148**, G99 (2001).

21. Y. J. Seo, S.-Y. Kim, and W.-S. Lee, *Microelectron. Eng.*, **65**, 371 (2003).
22. G. B. Basim, J. J. Adler, U. Mahajan, R. K. Singh, and B. M. Moudgil, *J. Electrochem. Soc.*, **147**, 3523 (2000).
23. R. Biswas, Y. Han, P. Karra, P. Sherman, and A. Chandra, *J. Electrochem. Soc.*, **155**, D534 (2008).
24. D. Rosales-Yeomans, T. Doi, M. Kinoshita, T. Suzuki, and A. Philipossiana, *J. Electrochem. Soc.*, **152**, G62 (2005).
25. W. F. Preston, *Trans. Opt. Soc., London*, **27**, 181 (1926).
26. T. K. Doy, K. Seshimo, K. Suzuki, A. Philipossiana, and M. Kinoshita, *J. Electrochem. Soc.*, **151**, G196 (2004).
27. H. Liang and D. Craven, *Tribology in Chemical Mechanical Planarization*, Taylor & Francis, New York (2005).
28. A. K. Sikder, F. Giglio, J. Wood, A. Kumar, and M. Anthony, *J. Electron. Mater.*, **30**, 1520 (2001).
29. D. DeNardis, J. Sorooshian, M. Habiro, C. Rogers, and A. Philipossian, *Jpn. J. Appl. Phys., Part 1*, **42**, 6809 (2003).
30. Y. Yamada, M. Kawakubo, O. Hirai, N. Konishi, S. Kurokawa, and T. Doi, *J. Electrochem. Soc.*, **155**, H569 (2008).