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Low-voltage and short-channel pentacene field-effect transistors with top-contact geometry using parylene-C shadow masks

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We have fabricated high-performance top-contact pentacene field-effect transistors using a nanometer-scale gate dielectric and parylene-C shadow masks. The high-capacitance gate dielectric, deposited by atomic layer deposition of aluminum oxide, resulted in a low operating voltage of 2.5 V. The flexible and conformal parylene-C shadow masks allowed fabrication of transistors with channel lengths of L=5, 10, and 20 μm. The field-effect mobility of the transistors was $\mu=1.14$ (± 0.08) $cm^2/V\,s$ on average, and the I_{MAX}/I_{MIN} ratio was greater than 10^6. © *2010 American Institute of Physics*. [doi:10.1063/1.3336009]

Organic electronics has attracted favorable attention in large-area applications including flexible circuits,[1,2] light-emitting diodes,[3] solar cells,[4] and sensors.[5] The field-effect mobility of several organic materials exceeds that of hydrogenated amorphous silicon,[6] and their low processing temperature makes them more attractive.

A nanometer-scale gate dielectric with high capacitance is required for making field-effect transistors (FETs) that can operate at low voltages suitable for portable electronic applications. Previously, a variety of methods were used to achieve high-capacitance gate dielectrics: oxidized aluminum,[7] solution-processed hafnium oxide,[8] polyvinyl alcohol,[9] and ion-gel dielectrics.[10] However, problems still remain such as the control of dielectric thickness and the existence of trap states. Atomic layer deposition (ALD) of aluminum oxide (AlO_X) is a good choice for organic FETs (OFETs) because the thickness of the deposited dielectric can be precisely controlled and defect-free dielectric films can be grown with optimized processing conditions. Previously, ALD of AlO_X was used in pentacene OFETs,[11,12] but those OFETs used thick dielectric films on the order of hundreds of nanometers, which resulted in high operating voltages of more than 10 V.

In the fabrication of OFETs, top-contact devices where source and drain electrodes are deposited on the organic semiconductor are preferred over bottom-contact devices. Bottom-contact devices generally have higher contact resistance, which reduces output current, due to poor growth of organic semiconductors on metal electrodes.[6] Although photolithography can be used to pattern metal electrodes on the organic semiconductor,[13] the top-contact devices are typically fabricated via evaporation through metal shadow masks to avoid degradation of the semiconductor layer. However, the metal shadow masks have several limitations, such as large feature sizes greater than 25 μm, rigidness, and difficulty in alignment. Recently, flexible and transparent parylene-C shadow masks have been used for patterning of biomolecules on polystyrene, glass, and PDMS substrates.[14] Due to their good adhesion on a variety of surfaces, patterns with features as small as 4 μm have been demonstrated with high reproducibility. The channel length affects a large number of device parameters, such as drain current, gate delay, and power dissipation, and FET performance is maximized with a shorter channel length.[15] Therefore, the small feature sizes and high yield of the parylene-C masks are advantageous in the fabrication of top-contact OFETs.

In this work, we used a nanometer-scale AlO_X gate dielectric deposited by ALD to achieve low-voltage operation and flexible parylene-C shadow masks to pattern gold electrodes whose distance was less than 10 μm. We demonstrated high-mobility and low-voltage pentacene transistors with short channel lengths as small as 5 μm.

A heavily doped n-type silicon wafer (<0.005 Ω cm) was used as a bottom-gate electrode. Trimethylaluminum and ozone were used as the source materials in the ALD process, where 45 ALD cycles were repeated at 350 °C. After the ALD process, the wafer was immersed into an octadecylphosphonic acid [OPA, $CH_3(CH_2)_{17}PO(OH)_2$] solution (3 mM in ethanol) to form a densely packed self-assembled monolayer (SAM) on the AlO_X. Hydrophobic alkane SAMs are known to reduce interfacial trap states and to increase the crystallinity of organic semiconductor layer. The OPA SAM was characterized by contact angle and ellipsometry measurements. The water contact angle of AlO_X was 9° while that of the OPA layer was 106°, due to the dense OPA SAM. The ellipsometry thicknesses of the AlO_X and the OPA layers were 45.7 (± 0.2) Å and 18.7 (± 0.4) Å, respectively. Test capacitors were made by a thermal evaporation of 100 nm-thick gold electrodes (on the order of 10^{-4} cm^2) on the OPA/AlO_X and AlO_X samples. As shown in Fig. 1, the maximum leakage current of the OPA/AlO_X sample was 0.47 $\mu A/cm^2$ when 3 V was applied, indicative of a pinhole free dielectric film. This value is comparable to the data from previously reported high-capacitance and low-leakage gate dielectrics.[7,8] The capacitance values of the OPA/AlO_X and AlO_X samples were 488.8 (± 4.5) nF/cm^2 and 804.1 (± 8.8) nF/cm^2, respectively.

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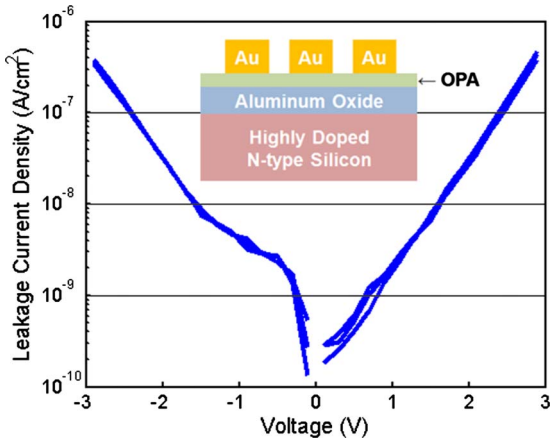

FIG. 1. (Color online) Leakage current density as a function of applied voltage on the gold electrodes.

On the prepared OPA/AlO_X/Si sample as gate dielectric and gate electrode, pentacene molecules were thermally evaporated with a substrate temperature of 60 °C in a vacuum chamber. The thickness of the pentacene layer was 45 nm, measured with a quartz crystal monitor. Finally, gold source/drain electrodes (40 nm) were thermally evaporated and patterned on the pentacene layer using 10 μm-thick parylene-C shadow masks. The fabrication of the parylene shadow masks was described in a previous publication.[14] The gold electrodes on the pentacene layer had channel lengths L=5, 10, and 20 μm, and the channel width to length ratio was fixed at 20. As shown in Fig. 2, all channel lengths were

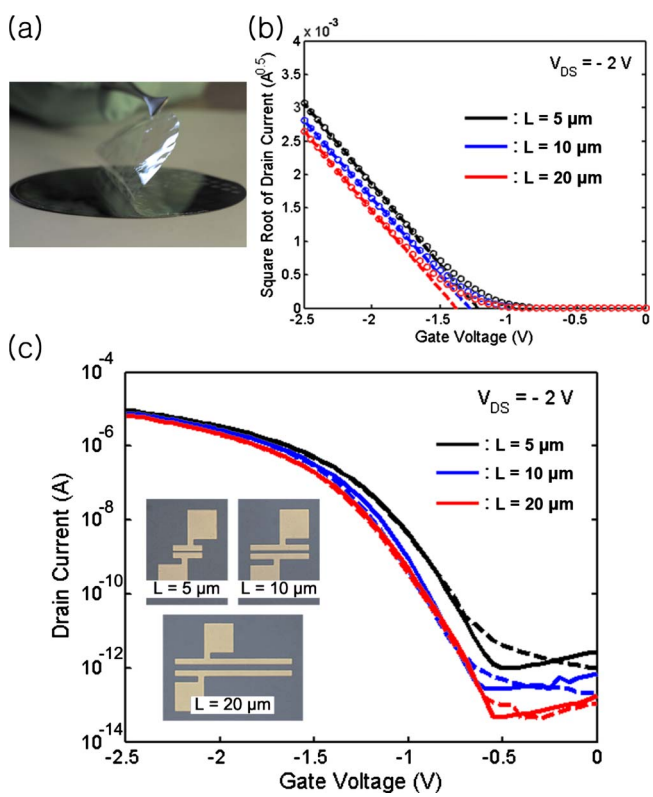

FIG. 2. (Color online) (a) The parylene-C shadow masks on a silicon wafer. (b) Square root of drain current vs gate voltage curves in the saturation regime. (c) Drain current vs gate voltage curves in the saturation regime and microscope images of the patterned gold electrodes on the pentacene. The gate voltage was swept from 0 to −2.5 V (solid lines) and immediately swept back from −2.5 to 0 V (dotted lines).

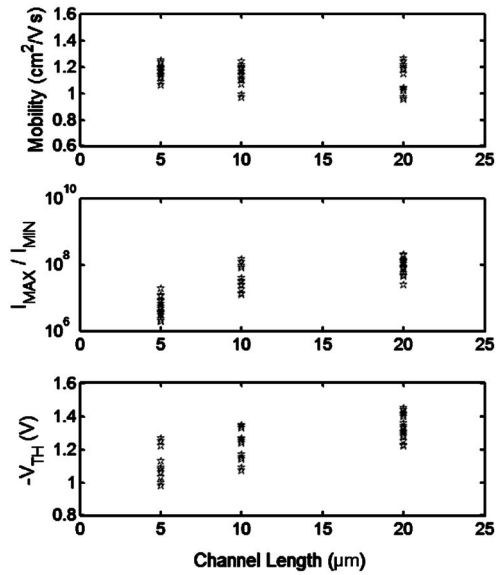

FIG. 3. Extracted device parameters in the saturation regime.

clearly defined due to a good adhesion of the parylene-C mask on the pentacene layer. Sixteen transistors were tested for each channel length in the saturation regime in air.

Figure 2 shows the drain current as a function of gate voltage in the pentacene OFETs with L=5, 10, and 20 μm in the saturation regime. Since the dense OPA SAM passivated the polar AlO_X surface and reduced the trap states, no hysteresis was observed in the on-state drain current. The average field-effect-mobility of our devices was μ=1.14 (±0.08) cm^2/V s for all the channel lengths, and this value is two to three times higher than the previous results from oxidized aluminum[7] and plasma-enhanced ALD of AlO_X on titanium.[12] The contact resistance, extracted by the transmission line method,[16] was 733 Ω cm, which is approximately 40% lower than the previous report with a similar device structure.[17] From the analysis of contact resistance, the limit of the channel length where the contact resistance becomes larger than the channel resistance was estimated between 1 and 2 μm. This high mobility, low contact resistance, and small limit of the channel length can be explained by the defect-free and ultrasmooth OPA/AlO_X gate dielectric, whose root-mean-square surface roughness was 0.2 nm, measured by AFM, and the use of top-contact electrodes.

The device parameters from each channel length are summarized in Fig. 3. The field-effect-mobility values had a similar distribution in each channel length while the I_{MAX}/I_{MIN} ratio and threshold voltage showed channel length dependence. As depicted in Fig. 2, the I_{MIN} significantly increased at shorter channel lengths. The magnitude of the threshold voltage in Fig. 3 gradually decreases as the channel length decreases. When the lateral electric field increases, the injection of charge carriers becomes easier between source/drain electrodes and the channel. Therefore, as the channel length shrinks, the subthreshold current increases, and the required gate voltage to turn on the transistors decreases. With the device structure in this work, the vertical electric field was much stronger than the lateral electric field, so a large variation in the threshold voltage with different channel lengths, observed in nanometer-scale silicon MOSFETs, did not occur.

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In conclusion, we have demonstrated short-channel pentacene OFETs with 2.5 V operating voltage by utilizing an ultrathin gate dielectric and flexible parylene-C shadow masks. The gate dielectric was made by a reproducible ALD process, allowing 2.5 V operation so that the OFETs can be used in portable applications. Rather than using photolithography, parylene-C shadow masks were used to pattern sub-10 μm channel lengths. The top-contact structure and shadow-mask process resulted in low contact resistance and high field-effect mobility. Our OFETs showed approximately 3.6 times higher field-effect mobility than previously reported short-channel and top-contact pentacene transistors fabricated by photolithography[13] and 1.4 times higher mobility than bottom-contact pentacene transistors.[18] In the near future, we aim to deposit AlO_X gate dielectric made by the ALD system on patterned metal gates,[19] so each transistor is individually controlled for the realization of electronic circuits.

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[1] H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid, and C. Dehm, IEEE Trans. Electron Devices **52**, 618 (2005).
[2] L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, Appl. Phys. Lett. **88**, 083502 (2006).
[3] N. K. Patel, S. Cinà, and J. H. Burroughes, IEEE J. Sel. Top. Quantum Electron. **8**, 346 (2002).
[4] S. H. Park, A. Roy, S. Beaupré, S. Cho, N. Coates, J. S. Moon, D. Moses, M. Leclerc, K. Lee, and A. J. Heeger, Nat. Photonics **3**, 297 (2009).
[5] M. E. Roberts, S. C. B. Mannsfeld, N. Queraltó, C. Reese, J. Locklin, W. Knoll, and Z. Bao, Proc. Natl. Acad. Sci. U.S.A. **105**, 12134 (2008).
[6] *Organic Field-Effect Transistors*, edited by Z. Bao and J. Locklin (CRC, Boca Raton, 2007).
[7] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, Nature (London) **445**, 745 (2007).
[8] O. Acton, G. Ting, H. Ma, and A. K.-Y. Jen, Appl. Phys. Lett. **93**, 083302 (2008).
[9] Y. Jang, D. H. Kim, Y. D. Park, J. H. Cho, M. Hwang, and K. Cho, Appl. Phys. Lett. **88**, 072101 (2006).
[10] J. H. Cho, J. Lee, Y. He, B. Kim, T. P. Lodge, and C. D. Frisbie, Adv. Mater. (Weinheim, Ger.) **20**, 686 (2008).
[11] X.-H. Zhang, B. Domercq, X. Wang, S. Yoo, T. Kondo, Z. L. Wang, and B. Kippelen, Org. Electron. **8**, 718 (2007).
[12] J. B. Koo, J. W. Lim, S. H. Kim, S. J. Yun, C. H. Ku, S. C. Lim, and J. H. Lee, Thin Solid Films **515**, 3132 (2007).
[13] C.-C. Kuo and T. N. Jackson, Appl. Phys. Lett. **94**, 053304 (2009).
[14] S. Selvarasah, S. H. Chao, C.-L. Chen, S. Sridhar, A. Busnaina, A. Khademhosseini, and M. R. Dokmeci, Sens. Actuators, A **145-146**, 306 (2008).
[15] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 1st ed. (Cambridge University Press, Cambridge, 1998).
[16] G. Horowitz, P. Lang, M. Mottaghi, and H. Aubin, Adv. Funct. Mater. **14**, 1069 (2004).
[17] H. Klauk, U. Zschieschang, and M. Halik, J. Appl. Phys. **102**, 074514 (2007).
[18] D. J. Gundlach, L. Jia, and T. N. Jackson, IEEE Electron Device Lett. **22**, 571 (2001).
[19] M. D. Groner, J. W. Elam, F. H. Fabreguette, and S. M. George, Thin Solid Films **413**, 186 (2002).

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