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Parallel arrays of individually addressable single-walled carbon nanotube field-effect transistors

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High-throughput field-effect transistors (FETs) containing over 300 disentangled, high-purity chemical-vapor-deposition-grown single-walled carbon nanotube (SWNT) channels have been fabricated in a three-step process that creates more than 160 individually addressable devices on a single silicon chip. This scheme gives a 96% device yield with output currents averaging 5.4 mA and reaching up to 17 mA at a 300 mV bias. Entirely semiconducting FETs are easily realized by a high current selective destruction of metallic tubes. The excellent dispersity and nearly-defect-free quality of the SWNT channels make these devices also useful for nanoscale chemical and biological sensor applications. © 2006 American Institute of Physics. [DOI: 10.1063/1.2161820]

I. INTRODUCTION

Carbon nanotubes¹⁻⁴ (CNTs) are arguably the best available material for realizing nano- and molecular-scale elec-tronics and sensor devices.^{5–7} The feasibility of single-walled carbon nanotube- (SWNT) based electronic devices, such as interconnects^{8,9} in molecular electronics, junction rectifiers,^{9–11} field-effect transistors (FETs),^{12,13} and logic gates,¹⁴ has been demonstrated in recent experiments. More recently, experiments demonstrating the use of SWNTs as the active channel in metal-oxide-semiconductor (MOS) FETs, which opens the possibility for a wide range of integrated CNT-complementary (C) MOS nanoelectronics, have also been reported.¹⁵ Despite these demonstrated breakthroughs, the progress toward CNT-based electronics has been rather slow due to a lack of (a) technique(s) to produce pure, isolated semiconducting SWNTs and (b) a process for an industrially scalable production of useful devices. Since most growth techniques yield a mixture of metallic (m) and semiconducting (sc) SWNTs, which are often difficult to separate, ingenious methods such as high electric-fieldinduced destruction^{16,17} and chemically modified deactivation^{18,19} of *m* SWNTs have been proposed and utilized to realize sc SWNT devices.

Assembly and fabrication of SWNT electronic devices still require several tedious steps just to realize a single or few functional devices, which do not conveniently lend themselves to high-yield productions. Some recent developments toward an industrially favorable SWNT transistor fabrication process include prepatterned catalysts where SWNTs selectively grow at the device sites, ^{20–24} and dispersing SWNTs over a surface in order to produce an entangled network.^{25,26}

In this paper, we report a three-step procedure that yields individually addressable arrays of high-throughput SWNT FETs. The simple approach described here could be easily integrated in the existing commercial processing of silicon electronics. The process flow involves (1) spin-casting a catalyst precursor polymer film on the substrate, (2) chemical vapor deposition (CVD) growth of SWNTs, and (3) metal electrode deposition. We take advantage of a recently reported CVD process²⁷ that yields highly dispersed, long strands (averaging 10 μ m in length) of nearly-defect-free single tube or thin uniform bundles (diameter, d \sim 1.5–4 nm) of pure SWNTs. The purity of SWNTs is confirmed by a weak D mode in the Raman spectrum.²⁷ SWNT density is optimized by controlling the polymer film thickness to create three to six tube bundles per 100 μ m², which provides a high density of separated and relatively disentangled tubes, therefore increasing the device sensitivity. A consistent and nearly uniform SWNT surface coverage in our approach allows for the direct deposition of metal electrodes onto the silica/nanotube surface without tedious positioning of the metal contacts or patterning of the catalyst to localize the nanotube growth.

Recently, there have also been reports^{25,26,28} of high output current CNT FETs that take advantage of multiple parallel nanotube channels between metal *source* and *drain* contacts. However, in these experiments, the channel-forming CNTs often appear in the form of an entangled network of junctions. In our method, individual, long, low-defect SWNT

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FIG. 1. (Color) Process flow for SWNT growth and device fabrication: step 1, spin coat catalytic polymer; step 2, perform CVD to synthesize SWNTs; and step 3, deposit Ti/Au electrodes through photolithography.

bundles form direct contacts with adjacent electrodes (7.5 μ m pitch) without a bridging tube network, thus reducing the effects of multiple junctions and scattering centers on carrier transport. The tube dispersity facilitates over 300 such direct connections in a single device and yields current values that are among the highest seen for SWNT devices: up to 17 mA was observed in these devices with 300 mV biases. Our approach allowed us to fabricate over 160 high output current SWNT devices on a single 15 × 15 mm² wafer in a simple three-step process.

II. EXPERIMENT

A schematic of the process flow for the SWNT growth and device fabrication is shown in Fig. 1. The SWNTs were directly grown²⁹ on a 1000 Å thermal oxide layer on a heavily doped (n-type) Si substrate which also served as the back gate. Au contacts (200 nm in thickness), serving as the source (S) and drain (D), were deposited on a Ti (20 nm in thickness) adhesion layer on the as-grown SWNT samples by photolithography. The electrodes were $100-\mu$ m-wide strips running the length of the sample (~ 15 mm) with an average separation distance of 7.5 μ m, as illustrated in Fig. 2, which gave ~160 devices on a single chip. Atomic force microscope (Digital Instruments Nanoman) imaging, performed in ambient conditions, was used to investigate the exact gap width and to locate bridging nanotubes between the Au strips. The sample was annealed at 200 °C in nitrogen for 30 min to improve electrode/nanotube interfaces and remove any process-induced oxide defects. Electrical measurements (Janis Cryo Probe with Keithley SCS 4200) were performed in vacuum at room temperature. Devices with observed gate dependence are termed semiconducting in nature and functional devices were determined by a detectable source-todrain current flow with an applied bias.



FIG. 2. (Color) (a) Single device design (top): SWNTs seen between Ti/Au (20/200 nm in thickness) electrodes on a highly doped silicon substrate with 1000 Å thermally grown oxide. The device width (gap) between electrodes is 7.5 μ m and the electrodes are 100 μ m in width running the length of the sample (~15 mm); (bottom) structure of entire sample which holds over 160 devices; (b) AFM phase image 11 × 11 μ m² showing a single nanotube bundle connecting the two gold pads.

III. RESULTS AND DISCUSSION

The atomic force microscope (AFM) images of the fabricated devices, Fig. 2(b), showed individual bundles of SWNTs, 1.5-4 nm in diameter, clearly bridging between Au electrodes. The SWNT bundles reach across the 7.5 μ m gap between contacts because they grow as long, straight tubes rather than short and curled, which would require multiple SWNTs overlapping one another in order to bridge a gap of this size. The devices (bridging SWNT gaps) were numbered sequentially. The AFM images of any gap performed at different locations showed several SWNT channels. In fact, from the measured output current (I) of the purely semiconducting devices, which averages 709 μ A with a 300 mV drain bias and using a previously reported³⁰ value of output current for a sc SWNT, we estimate that any gap contains between 375 and 750 nanotube bundles physically bridging the Au pads. This gives a maximum current value of 1.9–0.9 μ A carried by any single bundle at a 300 mV drain bias, which correlates with the previously reported value.³⁰

Two- and three-probe electrical measurements, which showed substantial contributions from metallic tubes even in



FIG. 3. (Color) Electrical map of devices 6-102. The blue lines represent the metallic devices and the red lines indicate semiconducting behavior. The current value is measured at 300 mV drain bias.

the dominantly sc SWNT bundles, were performed on 96 of the 160 devices (gaps) on the chip. The electrical response map of the tested devices is shown in Fig. 3, which indicates an average output current of 5.4 mA with a 300 mV drainto-source bias. Of the tested devices, 96% (92 devices) exhibited excellent electrical response, while 14% (13 devices) showed (Fig. 3) predominantly sc characteristics. The sc devices (red bars), as expected, are also characterized by their low conductivity compared to the metallic SWNT-dominated devices. Of the 13 sc devices, 7 showed strong gate dependence while the remaining 6 contained a mixture of *m* and sc responses.

It has been predicted³¹ that most CVD processes yield a higher percentage (~70%) of sc SWNTs. Accordingly, a higher percentage of our fabricated devices would be expected to exhibit sc characteristics. It is likely that our devices do have a higher percentage of sc SWNT bundles; however, the presence of even a small number of *m* SWNTs render the entire device metal like due to a very high drive current in the latter than the former. This could explain the observation of a rather larger number of dominantly metallic gaps (devices).

It is also clear that the fabricated devices give a high output current (hundreds of microamperes to tens of milliamperes) at fairly low bias voltages compared to that reported in previous studies.^{19,31} Although the presence of a small percentage of metallic tubes is evident based on three terminal measurements, the high-current response mainly results from *multiple* (parallel) channels in the device.³² The output $(I_{ds} \text{ vs } V_{ds})$ and the transfer $(I_{ds} \text{ vs } V_g)$ characteristics of a typical, purely sc device (gap 60) are shown in Fig. 4. The I_{on}/I_{off} ratio for device 60 (Fig. 4) at 100 mV is 4.35, which compares with the reported value of 2-4 for asfabricated devices consisting of multiple channels.^{17,28} It is worth noting that a value of $I_{\rm on}/I_{\rm off}$ up to 500 can be achieved in such devices, as shown by Seidel et al.,²⁸ after postfabrication treatment, such as selective destruction of metallic SWNTs by high electric field. Also, values as high as 10⁵ have been reported by Collins et al.,¹⁶ after such modifications to devices with initial $I_{\rm on}/I_{\rm off}$ ratios of ~3. Interestingly, our devices consistently show saturation of the output current below $V_g = -420 \text{ mV} (V_{on})$ at all bias voltages $(V_{ds}).$



FIG. 4. The output $(I_{ds} \text{ vs } V_{ds})$ characteristics of a sc SWNT FET (gap 60). The inset shows the transfer characteristics $(I_{ds} \text{ vs } V_g)$ of the device.

The transconductance, $g_m \left[= (dI_{ds}/d_{V_a})_{V_{ds}} \right]$ of a typical sc SWNT device in the study can be obtained from the estimated number of nanotube bundles and their average diameter. Taking an average "bundle" diameter, $d_{av} \approx 2.5$ nm, as obtained from AFM imaging and 300 channels (bundles) per gap, we estimate the transconductance $g_m = 236$, S/m at V_{ds} =100 mV over the entire gap for device 60.³³ For very short (200-300 nm) channel length devices, Wind et al.¹⁵ have reported a transconductance, $g_m \sim 2321$ S/m, suggesting that increasing the channel length of the SWNT FETs also potentially introduces scattering centers, thus reducing the transconductance of the devices. In contrast, the transconductance of the long channel-length devices fabricated in the present study compares quite favorably with those of the current *p*-type (*p*)-MOSFETs operating at ~ 100 S/m (Ref. 30) and offers potential applications in low-power highdensity electronics.

In contrast to the sc SWNT devices, a typical metaldominated device barely exhibited any gate dependence, as can be seen from Fig. 5 (inset) for a device identified as gap 46. Despite its metal-dominated behavior after fabrication, we were able to convert device 46 into an excellent FET by selective electric-field treatment,¹⁶ which imitated the purely semiconducting gap, 60. For this set of experiments, a 10 V back gate bias was applied in order to deplete the carriers (holes) in the sc SWNTs. A drain voltage was simultaneously swept to 2 V in order to surpass the breakdown voltage of the metallic nanotubes bridging gap 46. The current dropped



FIG. 5. The output (I_{ds} vs V_{ds}) characteristics after electric-field treatment of a predominantly metallic device (gap 46). The inset shows I_{ds} vs V_{ds} of the device before electric-field treatment.



FIG. 6. High electric-field-induced burning of metallic tubes in device 46: $V_g = 10 \text{ V}$, $V_{ds} = 0-2 \text{ V}$ sweep. Metallic SWNTs are destroyed at a V_{ds} of $\sim 1.4 \text{ V}$.

an order of magnitude around 1.4 V (drain), as shown in Fig. 6, suggesting destruction of the *m* SWNTs in the channel. After this selective destruction, lowering the gate voltage from 300 to -300 mV resulted in a 50.4% increase in current (Fig. 5), compared to a 7.69% increase prior to burning (Fig. 5 inset).

The dramatic increase in the gate-voltage dependence across the dominantly metallic device after high electric-field treatment suggests that the number of active sc devices on the chip can be further increased beyond the observed 14%.

IV. CONCLUSIONS

In summary, we have presented a simple three-step process for the fabrication of an array of over 160 devices on a single $(15 \times 15 \text{ mm}^2)$ chip. We have shown that 14% of the as-grown devices already function as FETs without any additional modifications to the SWNT bundles. The remaining devices with varying degrees of metallic contributions can be easily converted to purely sc transistors by electric-field treatment.¹⁶⁻¹⁹ The transconductance of the as-fabricated devices surpasses the current *p*-MOSFETs and can be further improved by a suitable treatment to remove metallic tubes in the channel. These desirable device properties offer a wide range of technological applications of the fabricated devices. Although considerable work is still needed toward materials and device processing, especially to improve semiconducting SWNT yield and controlled tube placement on a predesigned architecture, the approach described here can be easily adapted for batch processing to reliably fabricate highthroughput hybrid silicon-SWNT FETs. These devices are also optimally suitable for a wide variety of nanoscale sensing applications due to the natural tube dispersity, uniformity of the small-diameter bundles on the substrate surface, and clean, untangled bridging nanotubes in the channel.

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