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# Hardware Implementation of Image Space Reconstruction Algorithm using FPGA

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## Abstract

The Image Space Reconstruction Algorithm (ISRA) has been used in hyperspectral imaging applications to monitor changes in the environment and specifically, changes in coral reef, mangrove, and sand in coastal areas. This algorithm is one of a set of iterative methods used in the hyperspectral imaging area to estimate abundance. However, ISRA is highly computational, making it difficult to obtain results in a timely manner. We present the use of specialized hardware in the implementation of this algorithm, specifically the use of VHDL and FPGAs. The implementation of ISRA algorithm has been divided into hardware and software units. The hardware units were implemented on a Xilinx Virtex II Pro XC2VP30FPGA and the software was implemented on the Xilinx Microblaze soft processor. This case study illustrates the feasibility of this alternative design for iterative hyperspectral imaging algorithms. The main bottleneck found in this implementations was data transfer. In order to reduce or eliminate this bottleneck we introduced the use of blockrams (BRAMS) to buffer data and have data readily available to the ISRA algorithm.

## Goal

The goal of this research is to develop a hardware implementation of hyperspectral imaging algorithms with the objective to reduce the execution time. The use of FPGAs allows the flexibility of software while keeping the high processing speed of hardware implementations.

## State of the Art

- Rosario implemented the following abundance estimation methods: EMLL, ISRA, NNLS, NNLSO, NNSTO and CLSPSTO in software [3]. The main drawback of these implementations is their long running times.
- Parallel Independent Component Analysis (PICA), Independent Component Analysis (ICA), and K-means are some algorithms used in hyperspectral imaging implemented using FPGAs [1, 2, 4].
- In [1] Hongtao and Hairong implement a version of ICA called pICA. The implementation of ICA algorithm (for hyperspectral images reduction) in hardware provides an optimal parallelism environment and potential faster real time solution.
- In [2] Leeser and Theiler develop on FPGA the kmeans algorithm. This algorithm clustering pixels into classes, based on the spectral similarity of each pixel to other members of the class. FPGAs can provide a considerably speedup and are very flexible to allow testing of variants. The floating point libraries used for this implementation has been downloaded in [5].
- To the best of our knowledge, ISRA has not been implemented in hardware.

## Spectral Unmixing

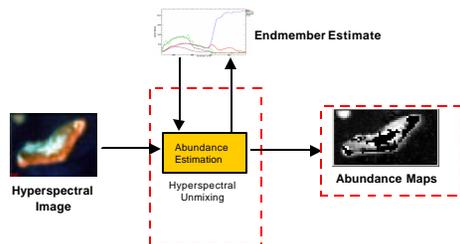


Figure 1. Unmixing Diagram Process

## Technical Approach

### Using Double Data Rate (DDR) Memory Interface

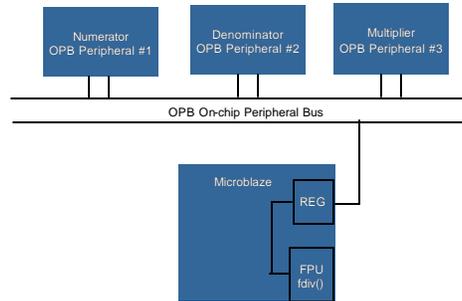


Figure 2. ISRA Architecture Diagram

### Using Double Data Rate (DDR) and BlockRAM (BRAM) Memory Interface

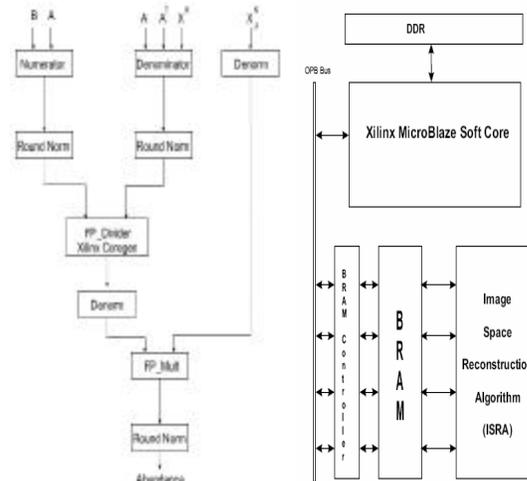


Figure 3. Complete ISRA Implementation and Architecture Diagram

## Image Space Reconstruction Algorithm (ISRA)

$$\hat{X}_j^{k+1} = \hat{X}_j^k \frac{\sum_{i=1}^m b_i a_{ij}}{\sum_{i=1}^m a_{ij} a_i^T \hat{X}^k}$$

Equation 1. ISRA Algorithm

## Software Implementation

The Microblaze is a processor designed by Xilinx that introduces an integrated single precision, IEEE-754 compatible Floating Point Unit (FPU). The MicroBlaze core is a 3-stage pipeline, 32-bit RISC Harvard architecture soft processor core with 32 general purpose registers, ALU, and an instruction set optimized for embedded applications. It supports both on-chip block RAM and external memory. A C program was created to send and receive data to and from the different units created in hardware. We used the floating point unit on Microblaze to make the floating point division required by ISRA algorithm. The C program and all VHDL codes were compiled by Xilinx compiling tools and downloaded into the FPGA.

## Results

- The ISRA algorithm was implemented using a Xilinx Virtex II Pro XC2VP30 FPGA.
- We demonstrated the feasibility of implementing hyperspectral analysis algorithms using FPGAs.
- Despite these results, the full design required more execution time than the original work presented in [3]. This was due to data transmission and Input/Output (I/O) bottlenecks. We are currently working to solve this problem.

## Technology Transfer

Hardware implementation of iterative hyperspectral imaging algorithms is important for two main reasons. First, a hyperspectral image is difficult to analyze in a timely manner due to its amount of information. Using hardware units such as FPGA's demonstrate the feasibility of this particular implementation in working with intensive computations and data movements. Second, hardware implementations can be used to perform real time unmixing. Having real time unmixing algorithms provides the capability of including computation units within sensors for instantaneous abundance estimations.

## Acknowledgement

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