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## Act 4 : A High-Precision, Multi-frequency Electrical Impedance Tomograph

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# ACT4: A High-Precision, Multi-frequency Electrical Impedance Tomograph.

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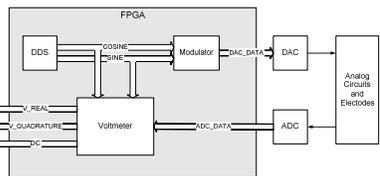
## Introduction:

- Electrical Impedance Tomography (EIT) forms images of the conductivity and permittivity of a body from electrical measurements made on its surface.
- Electrodes are placed on the surface of the volume to be imaged. Currents are applied to the electrodes. Voltages are measured on the electrodes.
- An image is reconstructed using knowledge of the electrode geometry, applied current data, and measured voltage data.

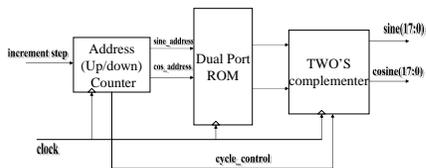
## System Design

- ACT4 is a multi-frequency Electrical Impedance Tomograph with firmware upgradeable digital components operating at discrete frequencies between 3 kHz to 1 MHz.
- 60 channels, each consisting of independent a voltage source, current source, current meter and voltmeter to obtain a high signal-to-noise ratio.
- A rack-mounted personal computer provides user I/O, instrument control, monitoring of safety systems, and data storage and retrieval.
- Four DSPs for real time reconstruction algorithm and one DSP for data flow control.
- One FPGA for a calibration board, one for a master board and 8 for the slave boards implementing the signal generator, modulator and the matched filter.
- The slave FPGA design has been modified (signal generator, matched filter length, sampling and the ADC clocks) to gain an increment in the SNR.

## One Channel Block Diagram



## Signal Generation



- The output frequency of the signal is determined by the increment factor for the address at the input.
- ROM is 18 bit wide, with a depth of 16384.

## Matched Filter

- A matched filter (MF) has the maximum output signal-to-noise ratio among all linear filters for a deterministic signal embedded in additive white noise.
- The MF structure can also be derived as a maximum likelihood estimator (MLE) assuming the dominant noise source is additive, white, and Gaussian.
- Defining the real and quadrature voltages as

$$V_r \equiv \sum_{k=1}^n y_k \cos\left(\frac{2\pi k}{n}\right)$$

$$V_q \equiv \sum_{k=1}^n y_k \sin\left(\frac{2\pi k}{n}\right)$$

- The amplitude and phase by solving the MLE problem is:

$$\hat{A} = \frac{2}{n} \sqrt{V_r^2 + V_q^2} \quad \hat{\phi} = \tan^{-1}(V_q/V_r)$$

- Another interpretation of this structure is as a coherent quadrature demodulator

## Complex Modulator

$$A \cos \alpha + B \sin \alpha = \sqrt{A^2 + B^2} \cos \left[ \alpha - \tan^{-1} \left( \frac{B}{A} \right) \right]$$

- By adjusting the factors A and B of the quadrature components, we can change the amplitude and phase of the output signal independently.
- One FPGA contains 8 modulators, producing signals at the same frequency but with different amplitude and phase, using a single DDS output.

## Oversampling Voltmeter

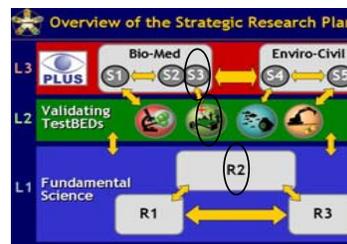
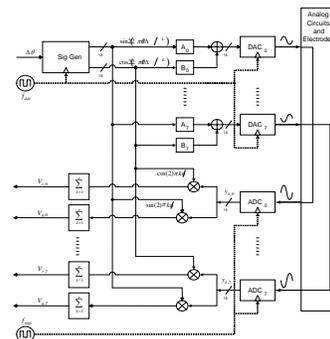
- Oversampling is used to increase the measurement precision beyond the ADC specification
- The MF output signal-to-quantization-noise ratio (SQNR) of the real channel is:

$$SQNR = 7.78 + 20 \log(\cos \phi / X_m) + 10 \log(4^{B+1} / \pi^2)$$

- The 3rd term means if we increase the total MF length n by a factor of 4, we could decrease the ADC precision requirement by 1 bit and still keep the SQNR unchanged.
- Undersampling scheme are also used to further ease the sampling rate requirement

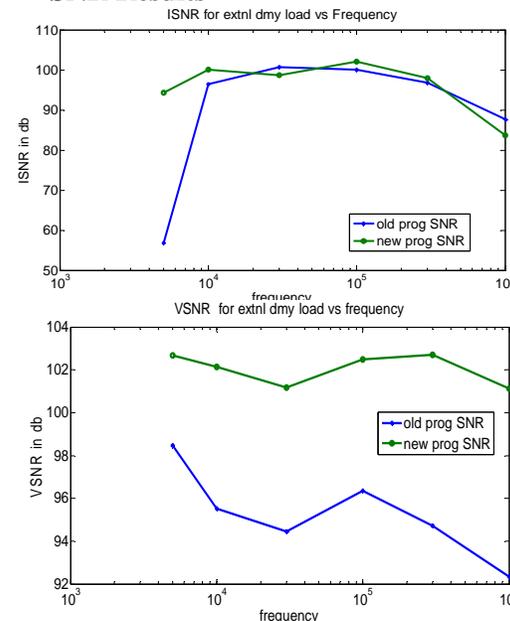
## FPGA Implementation

- The system includes one signal generator, 8 complex modulators, 8 matched filters and other blocks to control the analog circuits. It has been implemented in a two million gate Xilinx FPGA device (Virtex - II XC2V2000).



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## SNR Results



From the SNR plots, it can be observed that the ISNR shows a small improvement for the newer design and the VSNR shows a marked improvement and is approximately 10dB higher for the newer design at certain frequencies.

## Conclusion

- A multi-channel, discrete-frequency system has been designed for use in EIT.
- Modifications have been made on the existing slave FPGA design resulting in an increase in the SNR.
- Results have been obtained using an 8 channel external dummy load consisting of a resistive network.
- The new system has been verified by using results obtained from connecting the external dummy load and applying different sets of test patterns as the input.

## References:

### Publications Acknowledging NSF Support:

- Ning Liu, Gary J. Saulnier, J.C. Newell, D. Isaacson and T-J Kao. "ACT4: A High-Precision, Multi-frequency Electrical Impedance Tomography" Conference on Biomedical Applications of Electrical Impedance Tomography, University College London, June 22-24th, 2005.
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